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EXAMINER	
FERNANDEZ RIVAS, OMAR F	
ART UNIT	**PAPER NUMBER**
2129	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,835	NIELL ET AL.	
	Examiner	Art Unit	
	Omar F. Fernández Rivas	2129	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-22,33,35,37 and 48-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-22,33,35,37 and 48-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *A1, A2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to an AMENDMENT made by the Applicant entered on October 3, 2006.

2. The Office Action of June 29, 2006 is incorporated into this Final Office Action by reference.

Status of Claims

3. Claims 14, 16-22, 33, 35, 37, 48 and 49 have been amended. Claims 1-13, 23-32, 34, 36 and 38-47 have been cancelled. Claims 50-76 have been added. Claims 14-22, 33, 35, 37 and 48-76 are pending on this application.

Claim Objections

4. In light of the amendments made, the objection to claims 33-35, 37 and 48-49 made in the previous Office Action has been withdrawn.

5. Claims 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites the limitation "

determining a status of **the memory array** " in line 4. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 37 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim recites the limitation " ...receive input data in **the processing unit**" in line 15. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

9. In light of the cancellation of claims 26-31, the rejection under 35 USC 101 of the previous Office Action has been withdrawn.

10. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 14-22, 33, 35, 37 and 48-76 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The computer system must set forth a practical application of judicial exception to produce a real-world result. Benson, 409 U.S. at 71-72, 175 USPQ at 676-77. The invention is ineligible because it has not been limited to a substantial practical application.

For a claimed invention to be statutory the claimed invention must produce a useful, concrete, and tangible result. As the Supreme Court has made clear, " [a]n idea of itself is not patentable," *Rubber-Tip Pencil Co. v. Howard,* 20 U.S.

(1 Wall.) 498, 507 (1874); taking several abstract ideas and manipulating them together adds nothing to the basic equation. In re Warmerdam, 31 USPQ2d 1754 (Fed. Cir. 1994).

For a claimed invention to be statutory under 35 U.S.C. 101, the claims must have the FINAL RESULT (not the steps) produce a useful (specific, substantial, AND credible), concrete (substantially repeatable/ non-unpredictable), AND tangible (real world/ non-abstract) result.

The claims fail to provide a tangible result, and there must be a practical application, by either

1) transforming (physical thing) or

2) by having the FINAL RESULT (not the steps) achieve or produce a useful (specific, substantial, AND credible),concrete (substantially repeatable/non-unpredictable), AND tangible (real world/non-abstract) result.

A claim that is so broad that it reads on both statutory and non-statutory subject matter must be amended.

If the specification discloses a practical application but the claim is broader than the disclosure such that it does not require the practical application, then the claim must be amended. A claim that recites a computer that solely calculates a mathematical formula is not statutory.

In the present case, claim 14 describes a method that restores the value of a pointer in response to branch information. This is not a tangible result since this is only manipulation of data in a computer which is considered to be an

abstract idea since no real world result is obtained from moving data inside a computer. There is no data being processed and outputted in a way that provides a tangible (real world/non-abstract) result and a practical application from the method as claimed. A claim that can be read so broadly as to include statutory and nonstatutory subject matter must be amended to limit the claim to a practical application. In other words, if the specification discloses a practical application of a section 101 judicial exception, but the claim is broader than the disclosure such that it does not require a practical application, then the claim must be rejected (see MPEP 2106).

Claims 15-22 further describe the method of claim 14, but fail to provide the tangible result and practical application lacking on claim 14 and are rejected on the same basis.

Claim 37 describes a computer system. The claim describes the various components of the system. However, the claim fails to provide a practical application from the system as claimed. The claim only recites movement of data between processors and no output is generated and outputted so as to provide a practical application from the system. A claim that can be read so broadly as to include statutory and nonstatutory subject matter must be amended to limit the claim to a practical application. In other words, if the specification discloses a practical application of a section 101 judicial exception, but the claim is broader than the disclosure such that it does not require a practical application, then the claim must be rejected (see MPEP 2106).

Claim 48 describes a processor. The claim describes various components and operations of the processor. However, the claim fails to provide a tangible result from the operations performed by the processor. The claim only describes movement of data between memory locations which is not a real world (tangible) and practical result. No output is provided from the processor so as to provide a tangible (real world/non-abstract) result and a practical application from the processor as claimed. A claim that can be read so broadly as to include statutory and nonstatutory subject matter must be amended to limit the claim to a practical application. In other words, if the specification discloses a practical application of a section 101 judicial exception, but the claim is broader than the disclosure such that it does not require a practical application, then the claim must be rejected (see MPEP 2106).

Claim 49 further describes claim 48, but fails to solve the problems raised in regard to claim 48 and is therefore rejected in the same basis.

Claim 50 discloses an apparatus that retrieves a pointer value from a storage area based on branch information. This is not a tangible result since this is only manipulation of data in a computer which is considered to be an abstract idea since no real world result is obtained from moving data inside a computer. There is no data being processed and outputted in a way that provides a tangible (real world/non-abstract) result and a practical application from the apparatus as claimed. A claim that can be read so broadly as to include statutory and nonstatutory subject matter must be amended to limit the claim to a practical application. In other words, if the specification discloses a practical application of

a section 101 judicial exception, but the claim is broader than the disclosure such that it does not require a practical application, then the claim must be rejected (see MPEP 2106).

Claims 51-57 further describe the apparatus of claim 50, but fail to provide the tangible result and practical application lacking on claim 50 and are therefore rejected on the same basis.

Claim 58 describes a processor. The claim recites the components and their functions. However, the claim fails to provide a practical application. There is no result being outputted in a way so as to provide a practical application from the processor as claimed. A claim that can be read so broadly as to include statutory and nonstatutory subject matter must be amended to limit the claim to a practical application. In other words, if the specification discloses a practical application of a section 101 judicial exception, but the claim is broader than the disclosure such that it does not require a practical application, then the claim must be rejected (see MPEP 2106).

Claim 59-66 further limit claim 58, but fail to provide the practical application lacking in claim 58 and are therefore rejected on the same basis.

Claims 67-76 recite subject matter similar to that of claims 59-66. The claims also fail to provide a practical application from the invention as claimed, therefore claims 67-76 are rejected on the same basis as claims 59-66.

Claim Rejections - 35 USC § 103

11. The Applicant's arguments regarding the rejection under 35 USC 103 have been fully considered but are not persuasive.

In reference to Applicant's arguments:

Here, none of the criteria described in MPEP 2143 are satisfied since there is no motive to combine the references, the combination of references is physically impossible, and even if combined (which is impossible) the combination of references does not teach or suggest all the claim limitations. None of the references, alone and/or in combination teach receiving branch information, let alone branch information concerning branch resolution latency. Thus, none of the claims are obvious for at least this reason.

The combination of references does not teach receiving branch information. Additionally, there is no motive to combine, particularly in light of the teaching in Buck that no modifications to circuits interacting with the FIFO should be made. No motivation can be found to combine Buck (improve read access time for a FIFO) with Crouse, which describes itself as having "a primary purpose ... to provide a new processor instruction for enabling patch code segments to be provided which do not require the duplication in RWM of any good and valid ROM instructions." C6, L16-20.

Examiner's response:

It has been held that it is not necessary that the inventions of the references be physically combinable to render obvious the invention under review. Orthopedic Equipment Company, Inc. v. United States, 702 F.2d 1005, 1013, 217 USPQ 193, 200 (Fed.Cir. 1983); In re Andersen, 391 F.2d 953, 958, 157 USPQ 277, 281 (CCPA 1968); In re Sneed and Young, and E-Z Lay Pipe Corp. and Stream Line, Inc., 218 USPQ 385 (CAFC 1983).

In response to Applicant's argument that there is no motivation to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would

be motivated to make the proposed combination of references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is not what individual references themselves suggest but rather what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re Keller, 648 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983); In re McLaughlin, 170 USPQ 209 (CCPA 1971). References are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA 1969).

Regarding the arguments that the combination of references do not teach or suggest all the claim limitations, these have been addressed further below in this Office Action.

12. The arguments regarding claims 20-22 have been fully considered and are persuasive.

Claims 20-21

In reference to Applicant's Arguments:

Thus, none of these passages teach making a high threshold responsive to a maximum branch latency. The Office Action asserts that underflow and overflow are branch resolution latency. This is simply incorrect. Underflow and overflow as described in O'Connor are related to read and write rates to a stack, and are unrelated to branch resolution latency. For this additional reason this claim is not obvious and is in condition for allowance.

Examiner's response:

The Examiner acknowledges that the combined references do not teach that a high threshold level is responsive to the lesser of a maximum branch resolution latency and the low threshold level. Therefore the rejection of claim 20 under 35 USC 103 has been withdrawn. The rejection under 35 USC 103 of claim 21 has also been withdrawn based upon its dependence on claim 20. However, the claims are objected to as being dependent upon a rejected base claim.

Claim 22

In reference to Applicant's Arguments:

This claim depends from claim 20, which has been shown to be not obvious. Thus, this claim is similarly not obvious. Additionally, this claim describes that received information includes maximum branch latency and then characterizes maximum branch latency. This claim characterizes branch resolution latency as the number of instruction cycles to resolve a branch instruction in a processor. The Office Action asserts that Dally p1, P11 teaches that branch information includes branch resolution latency characterized as claimed. The passage defines branch latency. However, it fails to teach that this information is received in branch information available to the claimed method. Since the information is not received, the combination of references still fails to teach all the claimed elements. For this additional reason this claim is not obvious and is in condition for allowance.

Examiner's Response:

The test for combining references is not what individual references themselves suggest but rather what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re Keller, 648 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983); In re McLaughlin, 170 USPQ 209 (CCPA 1971). References are

evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA 1969). In the present case, receiving the information is taught by the combination of Buckenmaier, **Crouse** and O'Connor. The branch resolution latency taught by Dally can be included in the information taught by the combination of references to obtain the invention described by the Applicant.

However, the rejection under 35 USC 103 of claim 22 has been withdrawn based on its dependency of claim 20. The claim is objected to as being dependent upon a rejected base claim.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 14-17 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buckenmaier in view of Crouse et al. (US Patent #5,388,074, referred to as **Buckenmaier**; US Patent #4,831,517, referred to as **Crouse**).

Claim 14

Buckenmaier teaches a method comprising: processing one or more pop requests to read data from a FIFO memory (**Buckenmaier**: C1, L44-47; C3, L17-20; C4, L62-64; EN: reading when a read pointer signal is provided is processing a pop request).

Buckenmaier does not teach storing one or more prior pop pointer values of a pop pointer; receiving information to indicate at least one of the one or more pop requests was speculative and to indicate that a state of the pop pointer of the FIFO memory should be restored; and restoring one of the one or more prior pop pointer values to the pop pointer in response to the information.

Crouse teaches storing one or more prior pop pointer values of a pop pointer (**Crouse**: abstract; C12, L34-61; EN: a program counter is a pop pointer since it points to the next address in memory to read. The prior values are stored in the address register); receiving information to indicate at least one of the one or more pop requests was speculative and to indicate that a state of the pop pointer of the FIFO memory should be restored (**Crouse**: C2, L21-44; C5, L4-46; EN: Reading from the ROM is a pop request. Returning to the instruction following the patch hook (restoring a state of the pop pointer) if there is no corrective code means that the pop request was speculative) and restoring one of the one or more prior pop pointer values to the pop pointer in response to the information (**Crouse**: abstract; C12, L34-68, C13, L1-2; Fig. 7; EN: BAROA instructions contain the information).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Buckenmaier by incorporating storing prior values of a pop pointer and restoring a previous value of the pop pointer if a pop request was speculative as taught by Crouse for the purpose of allowing the system to recover from an incorrect branch instruction.

Claim 15

Buckenmaier does not teach the one or more prior pop pointer values of the pop pointer are stored into a pointer memory.

Crouse teaches the one or more prior pop pointer values of the pop pointer are stored into a pointer memory (**Crouse**: abstract; C12, L34-68, C13, L1-2; EN: the return address register is a pointer memory where the program counter value (pop counter) is stored).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Buckenmaier by incorporating storing prior values of the pop pointer in a pointer memory as taught by Crouse for the purpose of having means to retain values of the pointer so that the system can retrieve and use these values when necessary.

Claim 16

Buckenmaier does not teach restoring of the one prior pop pointer value to the pop pointer includes reading the one prior pop pointer value from the pop pointer memory, and loading the one prior pop pointer value into the pop pointer.

Crouse teaches restoring of the one prior pop pointer value to the pop pointer includes reading the one prior pop pointer value from the pop pointer memory, and loading the one prior pop pointer value into the pop pointer (**Crouse**: abstract, L19-27).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Buckenmaier by incorporating restoring the one prior pop pointer value to the pop pointer includes reading the one prior pop pointer value from the pop pointer memory, and loading the one

prior pop pointer value into the pop pointer as taught by Crouse for the purpose allowing the system to fetch the appropriate pop pointer value so that the pop pointer value can be changed to a value that achieves correct system performance.

Claim 17

Buckenmaier teaches prior to the processing of the one or more pop requests, storing data into a memory array of the FIFO memory, and incrementing a push pointer (**Buckenmaier**: C5, L6-29; C5, L56-61; Figs. 1 and 2; EN: in order to read data from a memory location, data must first be stored in it. Moving a write pointer to the next available register is incrementing a push pointer).

Claim 23

Buckenmaier does not teach bypassing the pop pointer and the push pointer, and directly addressing the memory array of the FIFO memory to read or write data thereto.

Crouse teaches bypassing the pop pointer and the push pointer, and directly addressing the memory array of the FIFO memory to read or write data thereto (**Crouse**: C5, L35-68, C6, L1-2; EN: unconditional branches bypass the push an pop pointers since a memory location different from the one currently addressed by the pop or push pointer is addressed).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Buckenmaier by incorporating bypassing the push and pop pointer to directly

address the memory as taught by Crouse for the purpose of not limiting the access to memory to the addresses pointed to by the push and pop pointers.

Claim 24

Buckenmaier teaches loading the pop pointer with an address of the memory array to randomly read data there-from (**Buckenmaier**: C1, L44-47; C5, L6-9; C9, L42-44; Fig 2; EN: making the read pointer address the first stage (memory location) is loading it with an address).

Claim 25

Buckenmaier teaches loading the push pointer with an address of the memory array to randomly write data thereto (**Buckenmaier**: C1, L44-47; C5, L9-10; C9, L38-41; Fig 2; EN: making the write pointer address the second stage (memory location) is loading it with an address).

Response to Applicant's arguments

15. The Applicant's arguments have been fully considered but are not persuasive.

Claim 14

In reference to Applicant's arguments:

The Office Action asserts that Crouse teaches receiving information to indicate at least one of the pop requests was speculative. The Office Action relies on C2, L21-44 and C5, L4-46 to support the assertion. However, C2, L21-44 simply describes how a branch instruction works, without describing the receipt of any branch information, let alone information that a branch was speculative. Similarly, C5, L4-46 simply describes how conventional patch hook processing includes unconditional branches, without describing the receipt of any branch information. While a pop pointer value may be stored and restored, the storing and/or restoring is unrelated to the receipt of any information, let alone the receipt of information indicating that a pop request was speculative.

Examiner's response:

The claims and only the claims form the metes and bounds of the invention. Limitations appearing in the specification but not recited in the claim are not read into the claim. The Examiner has full latitude to interpret each claim in the broadest reasonable sense. As can be seen in the sections cited, BAROA instructions contain information about the branch, like the memory address to access after the branch instruction.

Regarding the argument that no description is made as to whether a branch was speculative, the word "speculative" is not further defined in the claim or in the specification. Therefore, the Examiner considers that returning to the instruction following the patch hook if there is no corrective code means that the pop request was speculative, since the system assumed (speculated) that there was corrective code in that memory location. Moreover, if branches are taken unconditionally, they are being speculative.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buckenmaier and Crouse as applied to claim 14 above, and further in view of O'Connor (US Patent #6,532,531, referred to as **O'Connor**).

Claim 18

Buckenmaier and Crouse do not teach reading a pop pointer value of the pop pointer and a push pointer value of the push pointer, and determining a status of the memory array in response to the pop pointer value and the push pointer value.

O'Connor teaches reading a pop pointer value of the pop pointer and a push pointer value of the push pointer, and determining a status of the memory array in response to the pop pointer value and the push pointer value (**O'Connor**: C3, L19-65; C4, L1-8; C30, L31-58; Fig. 10A; EN: determining the fill and spill condition based on the optop and cache bottom pointers is determining the status of the memory).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Buckenmaier and Crouse by reading a pop pointer value and a push pointer value for determining the status of the memory as taught by O'Connor for the purpose of comparing the values of these pointers with the total memory available to decide if data can be read or written to a memory location.

Claim 19

Buckenmaier and Crouse do not teach the determining of the status of the memory array is further in response to a high threshold level and a low threshold level.

O'Connor teaches the determining of the status of the memory array is further in response to a high threshold level and a low threshold level (**O'Connor**: C3, L19-65; C4, L1-8; C30, L31-58; Fig. 10A).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of Buckenmaier and Crouse by determining the status of the memory based on a high threshold level and a low threshold level as taught by O'Connor for the purpose of having some means to measure when the memory is full or empty to decide if more data can be stored or read from the memory.

Response to Applicant's Arguments

In reference to Applicant's Arguments:

O'Connor describes a memory architecture that improves the speed of method invocation by storing method frames of method calls in two different memory circuits (Abstract). O'Connor uses stacks for the memory circuits. (Abstract). While stacks use push and pop operations, stacks are not FIFO (first-in first-out) memories. Rather they are FILO (first-in last-out) memories. Thus, any proposed combination of Buck and O'Connor is impossible and therefore there is no motive to combine these references. If the references were combined, the result would be inoperative, yielding no expectation of success. Furthermore, the combination of references still would not teach receiving information to indicate that a pop request was speculative. For at least these reasons claims 18-21 are not obvious and are in condition for allowance.

All of these passages, and indeed all of O'Connor describe stack operations, which simply cannot be added to the FIFO processing of Buck. While a push and pop pointer may be read, they are push and pop pointers for a stack and thus are not push and pop pointers as claimed. Even if combined, no information that indicates that a pop request was speculative is received.

Thus, there is no motive to combine the references, it is physically impossible to combine the references yielding no expectation of success, and even if combined the references still do not teach every element of the claim. For at least this reason claim 18 is not obvious and is in condition for allowance.

Examiner's Response:

Applicant cannot show non-obvious by attacking the references individually where as here the rejections are based on a combination of references see In re Keller USPQ 871 (CCPA 1981).

In response to Applicant's argument that any proposed combination of Buck and O'Connor is impossible and therefore there is no motive to combine these references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, there is no requirement that a motivation to make the modification be expressly articulated. The test for combining references is not what individual references themselves suggest but rather what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re Keller, 648 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Sernaker, 702 F.2d 989, 217 USPQ 1 (Fed. Cir. 1983); In re McLaughlin, 170 USPQ 209 (CCPA 1971). References are evaluated by what they suggest to one versed in the art, rather than by their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA 1969).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been

obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 50 and 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor et al. in view of Crouse et al. (US Patent #6,532,531, referred to as **O'Connor**; US Patent #4,831,517, referred to as **Crouse**).

Claim 50

O' Connor teaches an apparatus, comprising: a plurality of storage locations to store data (**O'Connor**: abstract, L1-13; C1, L41-45; Fig. 1); a pointer storage area to store one or more pointer values to index the plurality of storage locations (**O'Connor**: C3, L34-51; C26, L40-62).

O'Connor does not teach a control logic: to control storing a pointer value to the pointer storage area based, at least in part, on program branching information, and to control retrieving a pointer value from the pointer storage area based, at least in part, on program branching information.

Crouse teaches a control logic: to control storing a pointer value to the pointer storage area based, at least in part, on program branching information, and to control retrieving a pointer value from the pointer storage area based, at least in part, on program branching information (**Crouse**: abstract; C12, L34-68 to C13, L1-2; Fig. 7; Examiner's Note (EN): a program counter is a pointer stored in memory. BAROA instructions are branch information).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of O'Connor by storing a pointer

value and retrieving the pointer value based on branching information as taught by Crouse for the purpose of allowing the pointer to address a previous memory location after a branch instruction has been performed since computer instructions are stored sequentially in memory.

Claim 52

O'Connor does not teach the program branching information includes a branch flag to indicate a condition in which the one or more pointer values are to be read from the pointer storage area.

Crouse teaches the program branching information includes a branch flag to indicate a condition in which the one or more pointer values are to be read from the pointer storage area (**Crouse**: C12, L34-68; C13, L1-2; Fig 7; EN: an equality signal is a flag included in the branch information. The value of the program counter (pointer) is read from the register stack).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of O'Connor by incorporating a flag to indicate that the pointer value should be restored to a previous value as taught by Crouse for the purpose of allowing the system to decide if it should continue reading from the current memory location following the branch instruction or if it should continue reading from a memory location that was being read before the branch instruction was executed.

Claim 53

O' Connor teaches the program branching information corresponds to information speculatively read from one or more of the plurality of storage

locations (**O'Connor**: C6, L18-22; C8, L5-31; C101, L3-19; C18, L41-65; Figs. 1A and 1B; EN: fetching (reading) instructions from memory).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 51 and 54-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'connor and Crouse as applied to claim 50 above, and further in view of Buckenmaier (US Patent #5,388,074, referred to as **Buckenmaier**).

Claim 51

O'Connor and Crouse do not teach the one or more pointer values include a pop pointer to index data to be read from the plurality of storage locations and a push pointer to index data to be stored to the plurality of storage locations.

Buckenmaier teaches the one or more pointer values include a pop pointer to index data to be read from the plurality of storage locations and a push pointer to index data to be stored to the plurality of storage locations **Buckenmaier**: abstract, L10-13; C5, L6-14; Figs. 2, 4, 5 and 7; EN: a read pointer is a pop pointer and a write pointer is a push pointer as stated in page 1, paragraph 4 of the present application).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of O'Connor and Crouse by incorporating a pop pointer and a push pointer as taught by Buckenmaier for the purpose of allowing the system to keep track of the oldest information written and of the next available location into which the next information is to be written (**Buckenmaier**: C1, L44-48).

Claim 54

O' Connor teaches a status logic to indicate an amount of information stored in the pointer storage area (**O'Connor**: C3, L19-65; C4, L1-8; C30, L31-58; Fig 10A; EN: determining the fill and spill condition based on the optop and cache bottom pointers is an indication of the amount of data stored in memory).

Claim 55

O'Connor teaches the status logic to set a high status flag in response to the amount of information stored in the pointer storage area being greater than or equal to a high threshold level, and less than or equal to a maximum utilization level (**O'Connor**: C3, L19-65; C4, L1-8; EN: a spill condition is a high status flag).

Claim 56

O'Connor teaches the status logic to set a low status flag in response to an amount of information stored in the pointer storage area being less than or equal to a low threshold level, and greater than or equal to an empty threshold level (**O'Connor**: C3, L19-65; C4, L1-8; EN: a fill condition is a low status flag).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor and Crouse as applied to claim 50 above, and further in view of Dally et al (US Patent Publication #2003/0070059, referred to as **Dally**).

Claim 57

O'Connor does not teach the program branching information includes a branch resolution latency corresponding to a number of processor cycles to be used in resolving a conditional branch instruction.

Dally teaches the program branching information includes a branch resolution latency corresponding to a number of processor cycles to be used in resolving a conditional branch instruction (**Dally**: page 1, paragraph 11).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the combined teachings of O'Connor and Crouse by incorporating a branch resolution latency corresponding to a number of processor cycles to resolve a conditional branch instruction as taught by Dally for the purpose of having means to measure the delay in performing a set of instructions in a processor so that improvements can be made to reduce the delay.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 58-60, 63, 64, 67-69 and 72-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daniel et al. in view of Dally et al. (US Patent Publication #2001/0047439, referred to as **Daniel**; US Patent Publication #2003/0070059, referred to as **Dally**).

Claims 58 and 67

Daniel teaches a processor comprising: a plurality of processor cores (**Daniel**: page 1, paragraph 7, L1-1-12; page 4, paragraph 48, L1-12; page 8, claim 18, L1-5; Figs. 5-8; EN: the writer and the reader); a first plurality of first-in first-out (FIFO) memories to store data to be passed between the plurality of processor cores, wherein the first plurality of FIFO memories includes: a first input FIFO memory to store input data to be processed by at least one of the plurality of processor cores (**Daniel**: abstract; page 1, paragraphs 4-10; Fig. 2; EN: the writer passes data to the reader), and a first output FIFO memory to store output data to be output from at least one of the plurality of processor cores (**Daniel**: page 4, paragraphs 48; Fig.5; EN: the FIFO resides in the reader module and it outputs data when the reader module performs a read operation).

Dally teaches each of the processor cores including an instruction pipeline to speculatively execute instructions before a conditional branch is resolved (**Dally**: page 2, paragraph 13).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Daniel by incorporating an instruction pipeline to speculatively execute instructions before a conditional branch is resolved as taught by Dally for the purpose of allowing the processors to guess the outcome of a branch so as to reduce the processor's idle time due to the branch latency period (**Dally**: pages 1 and 2, paragraphs 12 and 13).

Claims 59, 68 and 73

Daniel teaches each FIFO memory includes: a push pointer storage area to store an address to which data is to be written (**Daniel**: page 1, paragraph 11, L1-4; Fig. 2).

Claims 60, 69 and 74

Daniel teaches each FIFO memory includes: a pop pointer storage area to store an address memory location from which data is to be read (**Daniel**: page 1, paragraph 11, L1-4; Fig. 2).

Claim 63

Daniel teaches each FIFO memory includes: a push pointer storage area to store an address to which data is to be written (**Daniel**: page 1, paragraph 11, L1-4; Fig. 2).

Claim 64

Daniel teaches each FIFO memory includes: a pop pointer storage area to store an address from which data is to be read (**Daniel**: page 1, paragraph 11, L1-4; Fig. 2).

Claim 72

Daniel teaches each FIFO memory includes a memory array to store data (**Daniel**: page 1, paragraphs 1-7).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 61, 62, 65, 66, 70, 71, 75 and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Daniel et al. in view of Dally et al. as set forth above and further in view of Crouse (US Patent #4,831,517, referred to as **Crouse**).

Claims 61, 70 and 75

Daniel does not teach each FIFO memory includes: a pointer memory to save one or more prior pop pointer values.

Crouse teaches each FIFO memory includes: a pointer memory to save one or more prior pop pointer values (**Crouse**: abstract; C12, L34-61; EN: a program counter is a pop pointer since it points to the next memory address in memory to read. The prior values are stored in the address register).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Daniel by incorporating a pointer memory to save one or more prior pop pointer values as taught by Crouse for the purpose of allowing the system to remember a prior value of the pointer so that it can address a previous memory location after returning from a branch instruction to continue program execution.

Claims 62, 71 and 76

Daniel does not teach each FIFO memory includes: control logic to retrieve one of the one or more prior pop pointer values in response to branch information.

Crouse teaches each FIFO memory includes: control logic to retrieve one of the one or more prior pop pointer values in response to branch information (**Crouse**: abstract; C12, L34-68 to C13, L1-2; Fig. 7; EN: a program counter is a pointer stored in memory. BAROA instructions are branch information).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Daniel by retrieving a prior pop pointer value as taught by Crouse for the purpose of allowing the pointer to address a previous memory location after a branch instruction has been performed since computer instructions are stored sequentially in memory.

Claim 65

Daniel does not teach each FIFO memory includes a pointer memory to store one or more prior pop pointer values.

Crouse teaches each FIFO memory includes a pointer memory to store one or more prior pop pointer values (**Crouse**: abstract; C12, L34-61; EN: a program counter is a pop pointer since it points to the next memory address in memory to read. The prior values are stored in the address register).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Daniel by incorporating a pointer memory to store one or more prior pop pointer values as taught by Crouse for the purpose of allowing the system to remember a prior value of the pointer so that it can address a previous memory location after returning from a branch instruction to continue program execution.

Claim 66

Daniel does not teach each FIFO memory includes: control logic to retrieve one of the one or more prior pop pointer values in response to branch information.

Crouse teaches each FIFO memory includes: control logic to retrieve one of the one or more prior pop pointer values in response to branch information (**Crouse**: abstract; C12, L34-68 to C13, L1-2; Fig. 7; EN: a program counter is a pointer stored in memory. BAROA instructions are branch information).

It would have been obvious to one of ordinary skill in the arts at the time of the applicant's invention to modify the teachings of Daniel by retrieving a prior pop pointer value as taught by Crouse for the purpose of allowing the pointer to address a previous memory location after a branch instruction has been performed since computer instructions are stored sequentially in memory.

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

28. Claims 14-22 and 48-76 have been rejected.

Correspondence Information

29. Any inquires concerning this communication or earlier communications from the examiner should be directed to Omar F. Fernández Rivas, who may be reached Monday through Friday, between 8:00 a.m. and 5:00 p.m. EST. or via telephone at (571) 272-2589 or email omar.fernandez rivas@uspto.gov.

If you need to send an Official facsimile transmission, please send it to (571) 273-8300.

If attempts to reach the examiner are unsuccessful the Examiner's Supervisor, David Vincent, may be reached at (571) 272-3080.

Hand-delivered responses should be delivered to the Receptionist @ (Customer Service Window Randolph Building 401 Dulany Street Alexandria, VA 22313), located on the first floor of the south side of the Randolph Building.

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Patent Examiner
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Friday, December 08, 2006

OFR

12/11/06
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SUPERVISORY PATENT EXAMINER